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METHOD AND DEVICE FOR TIME MEASUREMENT ON SEMICONDUCTOR MODULES EMPLOYING THE BALL-GRID-ARRAY TECHNIQUE

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METHOD AND DEVICE FOR TIME MEASUREMENT ON SEMICONDUCTOR MODULES EMPLOYING THE BALL-GRID-ARRAY TECHNIQUE

BACKGROUND

Field of the Invention

[0001] The invention relates to semiconductor measurements and more particularly to a method and a device for the time measurement of signals at pins or solder pads of semiconductor memory chips.

Background of the Invention

[0002] In semiconductor memory modules provided with registers, capacitive loads are buffered to a memory sub-channel bus and boosted again. A PLL circuit is used for refreshing a clock signal, while clocked buffer registers are used for refreshing command and address signals (CMD-ADR bus).

[0003] In order to maintain proper operation, it must be ensured that a clock signal reaches all parts of a memory module that relate the control of its timing to the system clock in a special time frame, that is, the PLL circuit itself, the registers, and DRAM semiconductor memory chips. For certain DDR memory modules that are operated with a differential clock signal at 133 MHz, the time frame is approximately -100 to +100 ps.

[0004] Since Process/Voltage/Temperature (PVT) variations of the parts concerned exert a strong influence on clock jitter of the PLL circuit and the amplification of the driving amplifiers, for each individual memory module the influence of loading of the DRAM semiconductor memory chips and the registers on the cut-off level of the positive and negative clock signals must be measured by a special time measurement technique to ensure that the clock signal arrives within the specified time frame.

[0005] In earlier conventional semiconductor chips, the leads or pins of which protrude laterally (for example so-called TSOP chip types), signals for time measurement mentioned above can be derived directly from the pins by means of a suitable measuring probe.

[0006] With the increasing operating speed of second generation DRAM memory modules (DDR-II modules), which operate at a clock frequency of up to 266 MHz, the so-called ball-grid-array (BGA) technique has been increasingly employed. The BGA technique produces better characteristic electrical values, including for example, smaller parasitic inductances. This type of chip packaging and contacting is used for PLLs, registers and DRAM chips, where all the pins lie under the chip body itself. In most cases the solder pads of the module (e.g., a DIMM board) that are assigned to the pins are located under the chip body itself, so that they cannot be reached by a measuring probe, or can be reached only with the aid of certain auxiliary measures, for time measurement.

[0007] Previously, the following known methods have been employed to overcome these difficulties in the case of modules that are loaded or can be loaded with semiconductor chips using the ball-grid-array technique:

[0008] 1. On modules that are loaded with components on one side, in which the components are located only on one side of a printed circuit board, access to the signal lines can be ensured by a plated-through hole (via), which leads from a loaded side of the module to the other, unloaded side, and is arranged as close as possible to the terminal (ball) of the semiconductor chip that is to be tested. However, this method has the disadvantage that a mask protecting the plated-through hole has to be

removed before the measurement, so that the circuit design has to be split into a measurable part with open plated-through holes, and a part intended for sale with protected plated-through holes. Furthermore, semiconductor modules that are loaded with components on both sides cannot be measured in this way, since they do not have any space for the respective plated-through holes to the other side of the module.

[0009] 2. On semiconductor modules that are loaded with components on two sides, the layout is supplemented by special test points, which allow the measuring probe to have direct access. These test points must lie as close as possible to the solder pad of the pin concerned (ball) that is to be tested or measured. The disadvantage of this method is that not all relevant signals can be accessed, since very densely loaded modules with an extremely high conductor density do not have the additional space for these test points. Furthermore, the capacitive load is changed by the added test points and the short conductor connections to them.

[0010] Tests have shown that the two methods referred to above differ only very little with regard to their measuring accuracy.

[0011] 3. Another measure employed is that of soldering socket-like measuring adapters between the chip and the semiconductor module. This requires very great effort, and such adapters also appreciably influence the measured values.

[0012] 4. A final measure employs soldering so-called wire adapters between a signal pin of the semiconductor chip and an assigned solder pad on the semiconductor module. A measuring probe can pick up the signal that is to be measured at the free end of the wire. The wire adapter must have insulation on the underside, so that no unwanted connection to underlying conductor tracks is established. This method has

the disadvantage, however, that it cannot be used in the case of all chips on a module and that the heat produced during the soldering often destroys the wire adapter, which makes the entire module unusable.

[0013] In view of the foregoing, it will be appreciated that there is a need to further improve time measurements associated with modern semiconductor chip packaging.

SUMMARY

[0014] Embodiments of the present invention provide a time-measuring method and a simple and low-cost time-measuring device adapted for it so that harmful influences on signals to be measured can be suppressed; and the electrical properties of the time-measuring device are adapted to the specified characteristic values of the signal pin to be measured, and simple contacting by a suitable measuring probe is possible.

[0015] In an exemplary embodiment of the present invention, a time-measuring method involves spatially assigning an equivalent conductor pattern (ECP) to a signal pin or solder pad (both hereinafter also referred to as "inputs") to be measured. The ECP is integrated on the semiconductor module, and is loaded with passive components chosen such that, when the ECP is connected to the solder pad while the signal pin of the semiconductor chip is detached, an equivalent load circuit (ELC) resulting from the component loading simulates the characteristic electrical values specified for the signal pin with the semiconductor chip loaded and the ELC not connected. The time measurement is performed at the solder pad connected to the ELC with the signal pin of the chip detached.

[0016] According to another embodiment of the present invention, a time-measuring device for measuring signals at solder pads assigned to signal pins on a

semiconductor chip module, includes an ECP integrated on the semiconductor module. The ECP is spatially assigned to the signal pin or solder pad to be measured and can be connected to the latter. Preferably, the form and electrical properties of the ECP are adapted to the time-relevant characteristic electrical values specified for the signal pin with the semiconductor chip loaded with components. Preferably the test device includes an ELC, which is formed by loading the ECP with passive components so that, when connected to the solder pad with the signal pin of the semiconductor chip detached, the device simulates the time-relevant characteristic electrical values specified for the signal pin with the semiconductor chip loaded with components and the ELC not connected. In the above manner, time measurement can be performed at the solder pad connected to the ELC with the signal pin of the semiconductor chip detached.

[0017] In preferred embodiments, the time-measuring method and time-measuring device may be advantageously used for time measurement of DIMM boards that can be loaded with DRAMs or DDR-DRAMs using the ball-grid-array technique.

[0018] In view of the fact that it is necessary for a ground reference potential to be picked off from the semiconductor module for each signal that is to be derived by the measuring probe from a signal pin or an associated solder pad, a time-measuring device according to an embodiment of the present invention advantageously makes it possible by a special design of the ECP that, after loading of the same with components, an electrical connection can be established with a reference ground pad provided by the ECP and located at a short distance from the solder pad assigned to the signal to be measured.

[0019] The above and further advantageous features of embodiments of the present invention including a time-measuring method and a time-measuring device are clarified further in the description which follows which relates to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Figure 1 illustrates a schematic layout view of an ECP, which is integrated on a semiconductor module board in spatial assignment to a designated signal pin (or its solder pad) that is to be measured and a reference ground pin or its solder pad.

[0021] Figure 2 schematically depicts an example of an equivalent circuit which shows components with which the ECP shown in Figure 1 can be loaded, in order to produce an ELC for a DRAM designated signal pin.

[0022] Figure 3 schematically depicts a plan view of a ball-grid-array layout which is provided on a semiconductor module for the mounting of a chip using the ball-grid-array technique and in which various possible positions of the ECP shown in Figure 1 are indicated.

[0023] Figure 4 schematically illustrates a measuring probe provided with a reference ground needle for the contacting of the signal and reference-ground solder pads according to Figures 1-3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0024] The following list of reference symbols is used consistently in the discussion to follow.

1	ECP
1'	ELC
2	signal pin/solder pad

3	ground pin/solder pad
5	measuring probe
11 - 22	solder pads of the ECP 1
R1, R2, R3, C1, C2, L	passive components
M	semiconductor module
a - d	spatial arrangements of the ECP 1

[0025] Figure 1 schematically depicts a view of a layout of an ECP that is integrated on a semiconductor module 100 and comprises a series of expediently arranged solder pads 11 - 22 and, if appropriate, connecting portions of conductor between the solder pads 11 – 22. The ECP can be loaded, for example, with the equivalent components shown in Figure 2 in order to form an ELC 1', which simulates the time-relevant electrical properties of a signal pin at which a time measurement is to be performed. ECP 1 is located in the direct vicinity of a signal pin (ball) that is to be measured (not shown) or its solder pad 2, and a reference ground pin or associated solder pad 3 on the semiconductor module 100. The low-impedance electrical connection of the ECP 1 shown in Figure 1, or ELC 1' may be fixedly provided, or may be established by small pieces of conductor that are subsequently soldered on during the loading of the ECP 1 with components. The same applies to the short pieces of conductor (depicted by dashed lines) between the individual solder pads 11 - 22 of the ECP 1.

[0026] According to Figure 1, the illustrated arrangement of solder pads 11 - 22 forms a first and a second longitudinal branch, from solder pads 11 - 14 on the one hand, and 17 - 20 on the other hand. In addition, a first and a second transverse branch, respectively comprise solder pads 15, 16 and 21, 22. The first transverse branch, comprising solder pads 15 and 16, branches between the second and third

solder pads 12, 13 and 18, 19 of the first and second longitudinal branches, respectively, while the second transverse branch adjoins the respective fourth solder pads 14, 20 of the first and second longitudinal branches.

[0027] Shown in Figures 1 and 2 is an example of how ECP 1 shown in Figure 1 can be loaded with passive components 30 (R1), 32 (R2), 34 (R3), 36 (L), 38 (C1) and 40 (C2) to produce an ELC 1', which simulates the electrical properties of a signal pin or the assigned solder pad of a DRAM chip at which a time measurement is to be performed. The component loading shown in Figure 2 is merely given by way of example and is not in any way to be considered as restrictive. The ECP shown in Figure 1 is so flexible that virtually any time-relevant characteristic value of signal pins of DRAM semiconductor memory chips and of other semiconductor chips can be simulated. In this way, ELC 1' loaded with the components shown in Figure 2, substitutes for a signal pin of a semiconductor chip, in particular a DRAM memory chip, that is to be measured, and advantageously also makes possible a spatially close and electrically low-impedance reference ground connection.

[0028] Figure 3, which shows a schematic plan view of a portion of a module 100' adapted for the mounting of a semiconductor chip, in particular a DRAM memory chip, merely illustrates by way of example various possible positions a - d at which the ECP 1 shown in Figure 1 can be integrated on module 100'. From the aspect of the layout of the ECP 1 on semiconductor module 100', the only requirement is that it must lie in the direct vicinity of the signal pin to be measured or its solder pad 2, and of a pad 3 carrying reference ground, in order that the distance of the connection between the solder pads 11 and 17 and solder pads 2 and 3 is as short as possible. For

example, as illustrated in Figure 1, the distance of the connection between the solder pads 11 and 17 and solder pads 2 and 3 is significantly less than the separation of signal pad 2 from reference ground pad 3. For a time measurement at designated signal pins or associated solder pads carrying high-frequency clock signals, the spatial proximity of solder pad 3 carrying a reference ground, as made possible by the ECP 1 according to the invention, provides an exact time measurement not possible without such a ground reference point. Figure 3 also shows that ECP 1 is integrated on semiconductor module 100' and is connected to solder pad 2 by the corresponding short conductor link between it and the first solder pad 11 or by the loading with the first resistor R1.

[0029] In an embodiment of the present invention for time measurement, the entire semiconductor chip is detached from the module 100' before or after ECP 1 is loaded with components to produce ELC 1' shown in Figure 2 or another ELC 1' adapted to the time-relevant electrical properties of the designated signal pin or associated solder pad. Alternatively, only the designated signal pin may be detached. If appropriate, the electrical connection of ECP 1' to solder pad 2 assigned to the detached signal pin is also established. Subsequently, time measurement takes place at solder pad 2, connected to ELC 1', with respect to the reference ground lying at reference ground solder pad 3. By changing the values of the ELC 1' or the component loading of ECP 1, all the times which can occur as a result of the PVT variation of a DRAM can be specified and simulated, and semiconductor module 100' can be adjusted to an optimum value without measurement of different PVT materials of the DRAM.

[0030] Figure 4 schematically shows a signal pickup at solder pad 2 and the associated reference ground pad 3 by an adapted measuring probe 5, where solder pad 2, which, for example, carries a clock signal, and where reference ground solder pad 3 are both connected to an ELC 1', designed, for example, according to Figure 2.

[0031] A time measurement can still be carried out at a semiconductor chip soldered on semiconductor module 100', since the ELC can be connected to the solder pad concerned in an electrically disconnectable manner. Furthermore, previously conventional test points can still be provided on the semiconductor module, so that a time measurement can also be performed at the latter test points.

[0032] As mentioned above, embodiments of the present invention provide, in particular, for time measurements on semiconductor modules, for example DIMM modules, which have semiconductor memory chips, registers and PLL chips mounted by means of the BGA technique and operate at a high clock frequency. Convenient access by a measuring probe to the signal pins that are to be measured is provided and falsification of measurement results or unreliable signal pickup from the signal pins in the case of BGA chips, can be eliminated.

[0033] The foregoing disclosure of the preferred embodiments of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many variations and modifications of the embodiments described herein will be apparent to one of ordinary skill in the art in light of the above disclosure. The scope of the invention is to be defined only by the claims appended hereto, and by their equivalents.

[0034] Further, in describing representative embodiments of the present invention, the specification may have presented the method and/or process of the present invention as a particular sequence of steps. However, to the extent that the method or process does not rely on the particular order of steps set forth herein, the method or process should not be limited to the particular sequence of steps described. As one of ordinary skill in the art would appreciate, other sequences of steps may be possible. Therefore, the particular order of the steps set forth in the specification should not be construed as limitations on the claims. In addition, the claims directed to the method and/or process of the present invention should not be limited to the performance of their steps in the order written, and one skilled in the art can readily appreciate that the sequences may be varied and still remain within the spirit and scope of the present invention.